AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor memory device comprising:

a memory cell comprising first and second data storage nodes, wherein the memory cell comprises:

a first inverter circuit including an input allocated to the second data storage node and an output allocated to the first data storage node, and a second inverter circuit including an input allocated to the first data storage node and an output allocated to the second data storage node; and

first access means connected to the first data storage node for reading out data, and storage control means serially connected to a drive transistor of the second inverter circuit.

2. (Original) A semiconductor memory device according to claim 1, wherein the memory cell further comprises second access means for accessing the second data storage node, the second access means being activated with a write signal thereby performing data transfer between a write bit line and the second data storage node.

3. (Original) A semiconductor memory device according to claim 2, wherein the first access means is activated with a memory access signal thereby performing data transfer between a read and write bit line and the first data storage node.

4. (Original) A semiconductor memory device according to claim 3, wherein the first and second inverter circuits forming the memory cell includes a CMOS inverter circuit and the first and second access means and the storage control means include NMOS transistors.

5. (Original) A semiconductor memory device according to claim 1, wherein the memory cell further comprises second access means for accessing the second data storage node and the second access means is activated by a write signal to reset the second data storage node.

6. (Original) A semiconductor memory device according to claim 5, wherein the first and second inverter circuits forming the memory cell includes a CMOS inverter circuit and the first and second access means and the storage control means include NMOS transistors.

7. (Currently Amended) A semiconductor memory device comprising:

a memory cell comprising first and second data storage nodes, wherein the memory cell comprises:

a first inverter circuit including an input allocated to the second data storage node and an output allocated to the first data storage node, and a second inverter circuit including an input allocated to the first data storage node and having an output allocated to the second data storage node; and

a first access ~~means~~ transistor connected to the first data storage node for reading out data, and a transistor serially connected to a drive transistor of the second inverter circuit.

8. (Currently Amended) A semiconductor memory device according to claim 7, wherein the memory cell further comprises second access ~~means~~ transistor for accessing the second data storage node and the second data storage node is activated by a write signal to perform data transfer between a write bit line and the second data storage node.

9. (Currently Amended) A semiconductor memory device according to claim 8, wherein the first access ~~means~~ transistor is activated by a memory access signal to perform data transfer between a read and write bit line and the first data storage node.

10. (Currently Amended) A semiconductor memory device according to claim 7, wherein the memory cell further comprises second access ~~means~~ transistor for accessing the

second data storage node and the second data storage node is activated by a write signal to reset the second data storage node.

11. (Original) A semiconductor memory device comprising:

first and second data storage nodes;

a first inverter circuit including an input allocated to the second data storage node and an output allocated to the first data storage node, and a second inverter circuit including an input allocated to the first data storage node and including an output allocated to the second data storage node; and

a first access transistor connected to the first data storage node for reading out data, and a transistor serially connected to a drive transistor of the second inverter circuit, wherein the transistor is turned off during reading of data from the first data storage node.

12. (Original) A semiconductor memory device comprising first and second inverter circuits connected in loop to form first and second data storage nodes, and first and second access means for accessing the first and second data storage nodes, and storage control means connected to a drive transistor of the second inverter circuit in series, wherein

the first access means is activated by a read signal to perform data transfer between a read bit line and the first data storage node and the second access means is activated by a write signal to perform data transfer between a write bit line and the second data storage node.

13. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, further comprising a sense amplifier including a bit line for transferring data to and from the memory cell, a data line for transferring data to and from an input and output circuit, an inverter circuit including an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the data line, and data write means activated by a write signal for transferring data from the data line to the bit line.

14. (Original) A semiconductor memory device according to claim 13, wherein the sense amplifier further comprises precharge means for precharging the bit line, and level-

maintaining means having an input applied with the output of the inverter circuit for maintaining a level of the bit line.

15. (Original) A semiconductor memory device according to claim 14, wherein the data line of the sense amplifier comprises a read data line connected to the read means, and a write data line connected to the write means.

16. (Original) A semiconductor memory device according to claim 14, wherein the sense amplifier further comprises write precharge means connected to a write bit line, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

17. (Original) A semiconductor memory device according to claim 15, wherein the sense amplifier further comprises precharge means connected to a write bit line, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

18. (Original) A semiconductor memory device according to claim 14, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

19. (Original) A semiconductor memory device according to claim 15, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and second write means for transferring inverted write data from an inverted write data line to the write bit line.

20. (Original) A semiconductor memory device according to claim 15, wherein the sense amplifier further comprises a write bit line connected to the output of the inverter circuit, and a write transistor having a gate input applied with a signal from the write data line, a source connected to a ground potential and a drain connected to the write bit line.

21. (Original) A semiconductor memory device according to claim 14, wherein the sense amplifier further comprises a write bit line connected to an inverted write data line.

22. (Original) A semiconductor memory device according to claim 15, wherein the sense amplifier further comprises a write bit line connected to an inverted write data line.

23. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, further comprising a sense amplifier which comprises a bit line and a write bit line for transferring data to and from the memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, data write means activated by a write signal for transferring data from the inverted write data line to the write bit line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line.

24. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, further comprising a sense amplifier which comprises a bit line and a write bit line for transferring data to and from the memory cell, a read data line and an inverted write data line for transferring data to and from an input and output circuit, an inverter circuit having an input allocated to the bit line, data read means for transferring an output of the inverter circuit to the read data line, precharge means for precharging the bit line, and level-maintaining means input with the output of the inverter circuit for maintaining a level of the bit line, wherein the write bit line is directly connected to the inverted write data line.

25. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, further comprising a sub word driver for selecting a read word line in response to a main word signal, a read block selection signal and an inverted read block selection signal and selecting a write word line in response to a main word line, a write block selection signal and an inverted write block selection signal.

26. (Original) A semiconductor memory device according to claim 25, wherein the sub word driver comprises a first inverter circuit having an input applied with the main word signal for outputting a read word line signal, and a first transistor having a drain applied with the read word line signal, wherein the first inverter circuit is formed between the read

block selection signal and a ground potential and the first transistor has a gate applied with the inverted read block selection and a source connected to a ground potential.

27. (Original) A semiconductor memory device according to claim 25, wherein the sub word driver comprises a second inverter circuit having an input applied with the main word signal for outputting a write word line signal, and a second transistor having a drain applied with the write word line signal, wherein the second inverter circuit is formed between the write block selection signal and a ground potential and the second transistor has a gate applied with the inverted write block signal and a source connected to a ground potential.

28. (Original) A memory cell comprising a plurality of elements, the memory cell being placed in layout within an L-shaped region.

29. (Original) A static random access memory comprising a static random access memory cell including a plurality of elements and placed in layout in an L-shaped region.

30. (Original) A semiconductor memory device comprising a memory cell including a plurality of elements and placed in layout in an L-shaped region.

31. (Original) A semiconductor memory device according to claim 30, wherein the memory cell comprises a static random access memory cell.

32. (Original) A semiconductor memory device according to claim 30, wherein the memory cell comprises P well regions formed on both sides of an N well region, and the N well region and the P well regions having one sides which are continuous with each other while sides opposing to the continuous sides are discontinuous thereby forming the L-shaped region in which one of the P well regions protrudes.

33. (Original) A semiconductor memory device according to claim 32, wherein a ground potential is extracted from a side of the P well region with a low height and a power supply potential is extracted from the N well region at a side contiguous to the side of the P well region.

34. (Original) A semiconductor memory device according to claim 30, wherein a memory cell array composed of the memory cells inverted in mirror in three directions,

respectively, has a central area formed with a vacant space in which none of elements forming the memory cells is disposed.

35. (Original) A semiconductor memory device according to claim 34, wherein the vacant space is defined in layout to allow elements forming a sense amplifier to be disposed.

36. (Original) A semiconductor memory device comprising a memory cell array including memory cells inverted in mirror in three directions, respectively, and disposed in a layout including a central area having a vacant space in which none of elements forming the memory cells are disposed and the vacant space has a layout in which elements forming a sense amplifier are placed.

37. (Original) A semiconductor memory device according to claim 36, wherein the sense amplifier includes an inverter circuit and a read transistor for transferring a cell data from a bit line to a data line during reading operation, and a write transistor for transferring data from a data line to the bit line during writ operation.

38. (Original) A semiconductor memory device according to claim 36, wherein the sense amplifier includes elements placed in layout in a vacant space of an adjacent memory cell region.

39. (Original) A semiconductor memory device according to claim 38, wherein the sense amplifier has wiring placed in layout in an adjacent memory cell region.

40. (Original) A semiconductor memory device according to claim 39, wherein the sense amplifier has wiring placed in layout in a part of an adjacent memory cell region at a power wiring area thereof.

41. (Original) A semiconductor memory device according to claim 36, wherein one piece of the sense amplifier is placed in layout for an N-piece (with N representing a multiple of 8) of memory cells.

42. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, wherein elements forming the memory cell are placed in layout in an L-shaped region.

43. (Currently Amended) A semiconductor memory device according to ~~claim 1~~ claim 2, wherein a memory cell array including memory cells inverted in mirror in three directions, respectively, has a central area formed with a vacant space in which no element forming the memory cell is disposed but elements forming a sense amplifier are disposed.

44. (Original) A semiconductor memory device according to claim 5, wherein elements forming the memory cell are placed in layout in an L-shaped region.

45. (Original) A method of performing a reading in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when a write word line of the memory cell is activated, the storage control means is turned off and the first access means allows a bit line and the first data storage node to be connected to each other to read a memory cell data on the bit line.

46. (Original) A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when read and write word lines of the memory cell are activated, the storage control means is turned off and the second access means resets the second data storage node to a low voltage potential while the first access means allows a bit line and the first data storage node to be connected to each other and, subsequently, the write word line is inactivated to allow a data of the bit line to be written to the first data storage node.

47. (Original) A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

when read and write word lines of the memory cell are activated, the storage control means is turned off and the first access means connects a bit line and the first data storage node to each other to allow a data of the bit line to be written to the first data storage node, and the second access means connects a write bit line and the second data storage node to each other to allow a data of the write bit line to be written to the second data storage node.

48. (Original) A method of performing a writing in a semiconductor memory device in which a memory cell comprises first and second inverter circuits connected in loop to form first and second data storage nodes, first and second access means accessing the first and second data storage nodes, respectively, and storage control means serially connected to a drive transistor of the second inverter circuit, wherein:

during an operation to perform writing to the memory cell, the storage control means is turned off and the second access means allows a write bit line and the second data storage node to be connected to each other to allow a data of the write bit line to be written to the second data storage node.